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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/613,271	KO ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-15* is/are allowed.

6)☒ Claim(s) *16,17,25-31,48 and 49* is/are rejected.

7)☒ Claim(s) *18-24 and 32-47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 03/21/05. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 16, 17, 25 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Clark et al. (USP 6639827).

As to claim 16, Clark et al.'s figure 4 shows a data latch apparatus, comprising: a first latch (130, 140) for latching a data signal (D); a second latch (200, 190) coupled to the first latch for retaining the data signal while the first latch is inoperative (standby or power down); a transfer device (170, 180) connected between the first and second latches for transferring the data signal between the first and second latches; the first latch including a first plurality of transistors (it is inherent that CMOS inverter includes plurality of transistors, column 2, line 67), each transistor of the first plurality having a gate oxide; the second latch including a second plurality of transistors, each transistor of the second plurality having a gate oxide that is thicker than said gate oxides of the first plurality of transistors; the transfer device including a transistor having a gate oxide that is thicker than the gate oxides of the first plurality of transistors; and the first latch further for latching the data signal independently of contemporaneous operating

characteristics respectively associated with the transistors of the second plurality and said transfer device.

As to claim 17, figure 4 shows that the transfer device includes a third plurality of transistors (170, 180) having respective gate oxides which are thicker than the gate oxides of the first plurality of transistors, the first latch further for latching the data signal independently of contemporaneous operating characteristics respectively associated with said transistors of said third plurality.

As to claim 25, figure 4 shows that the operating characteristics are conductance characteristics.

As to claim 26, figure 4 shows that the second latch is for retaining said data signal while said first latch is inoperative due to removal of power therefrom.

As to claims 27 and 28, Clark's figure 1 further shows data processing logic (20) for performing data processing operations; a plurality of registers (column 2, lines 67-67, teaches that the memory 30 comprises plurality of circuit figure 2 or 4) coupled to the data processing logic for storing data associated with the data processing operations.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clark et al. (USP 6639827).

Clark et al.'s figure 1 shows all limitations of the claims except for the circuit figure 1 is used in a wireless communication devices, such as mobile telephone, a laptop computer and a personal digital assistant. However, it is notoriously well known that such wireless communication devices comprise microprocessor or processor. Clark et al.'s processor has the benefit of low power consumption. Therefore, it would have been obvious to one having ordinary skill in the art to use Clark et al.'s processor in such wireless communication devices for the purpose of saving power consumption.

5. Claims 31, 48 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshi et al. (USP 6853239) in view of Krenik et al. (USP 4845675).

As to claim 31, Hoshi et al.'s figure 1 shows an apparatus comprising: a data signal input (DT) for receiving a data signal produced by a first logic device (11); a latch (32) coupled to the data signal input for retaining the data signal while the first logic device is inoperative, and circuit 12 coupled to the latch. Thus, figure 1 shows all limitations of the claims except for the detail of circuit 12. However, Krenik et al.'s figure 1 shows a data latch circuit that operable in high speed. Therefore, it would have been obvious to use Krenik et al.'s latch in circuit 12 for the purpose of latching or buffering the output of Hoshi et al.'s signal DT'. Thus, the modified Hoshi et al.'s figure 1 further shows a driver (Krenik et al.'s 22, 26, 28) coupled to the latch for, while the first logic device is inoperative, driving the data signal as retained in the latch to an input of a second logic device (the remain elements in Krenik's figure 1) that remains operative while the first logic device is inoperative.

As to claim 48, the modified Hoshi et al.'s figure 1 shows the driver is an inverter Driver (Krenik et al.'s 26)

As to claim 49, the modified Hoshi et al.'s figure 1 shows driver is for driving the data signal while the first logic device is inoperative due to removal of power therefrom.

Allowable Subject Matter

6. Claims 1-15 are allowed.

7. Claims 18-24 and 32-47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-15 are allowable because the prior art fails to teach or suggest that the second latch powered by a second power supply other than the first power supply.

Claims 18-20 and 24 would be allowable because the prior art fails to teach or suggest that second latch includes a first node for providing said data signal to the transfer device, the third plurality of transistors including first and second transistors having respective gates connected to the first node.

Claims 21-23 would be allowable because the prior art fails to teach or suggest that second latch includes first and second nodes for providing the data signal to the transfer device, the third plurality of transistors including first and second transistors having respective gates which are respectively connected to said first and second nodes.

Claims 32-47 would be allowable because the prior art fails to teach or suggest that an output coupled to the driver for providing the data signal to the input of the second logic device, and further including a further driver coupled to the data signal input and the output, the further driver for driving the data signal to the input of the second logic device while the first logic device is operative.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

April 27, 2005